IN THE CLAIMS:

1. (Currently amended) A data processing system which ~~may be situated~~ **is adapted to function** in a reduced-power mode, comprising a first data processing unit that has access to a memory belonging to the first data processing unit and a second data processing unit **having its own memory, said second data processing unit having** ~~that has~~ access to the memory belonging to the first data processing unit,

characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system **so that the second data processing unit utilizes the memory belonging to the first data processing unit instead of its own memory**.

2. (Previously presented) A data processing system as claimed in Claim 1,

characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a period of time in which the reduced-power mode of the data processing system implies a reduced-power mode of the first data processing unit.

3. (Currently Amended) A ~~data processing system as claimed in Claim 1~~,

A data processing system which may be situated in a reduced-power mode, comprising a first data processing unit that has access to a memory belonging to the

first data processing unit and a second data processing unit that has access to the memory belonging to the first data processing unit,

characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system, and

characterized in that the first data processing unit is arranged for offering the second data processing unit access to the memory belonging to the first data processing unit when a memory belonging to the second data processing unit is switched off.

4. (Previously presented) A system as claimed in Claim 1,

characterized in that the memory belonging to the first data processing unit forms part of the first data processing unit.

5. (Previously presented) A system as claimed in Claim 1,

characterized in that the memory belonging to the first data processing unit is a cache memory.

6. (Previously presented) A system as claimed in Claim 1,

characterized in that the first data processing unit is a microprocessor.

7. (Previously presented) A system as claimed in Claim 1,

characterized in that the second data processing unit is a video controller.

8. (Currently amended) A data processing unit having access to a memory belonging to the data processing unit which data processing unit may be situated in a reduced-power mode, characterized in that the data processing unit is arranged for offering access in the reduced-power mode to the memory belonging to the data processing unit **to a second data processing unit having a second memory unit of its own**.

9. (Currently Amended) A data processing system as claimed in Claim 8, further comprising a mechanism that allows the first data processing unit to offer ~~a~~ **the** second data processing unit access to the memory belonging to the first data processing unit in the reduced-power mode.

10. (Previously presented) A data processing system as claimed in Claim 9, wherein the second memory unit can be accessed by system components other than the first or second data processing units in the reduced-power mode.

11. (Currently amended) ~~**A data processing system as claimed in Claim 9,**~~

A data processing unit having access to a memory belonging to the data processing unit which data processing unit may be situated in a reduced-power mode, characterized in that the data processing unit is arranged for offering access in the reduced-power mode to the memory belonging to the data processing unit,

a mechanism that allows the first data processing unit to offer a second data processing unit access to the memory belonging to the first data processing unit in the reduced-power mode,

wherein the first data processing unit is arranged for offering the second data processing unit access to the first memory when the second memory is switched off.

12. (Previously presented) A data processing system as claimed in Claim 9, wherein that the memory belonging to the first data processing unit is a cache memory.

13. (Currently amended) A data processing system which may be situated in a reduced-power mode having a first data processing unit that has access to a first memory associated with the first data processing unit and a second data processing unit that has access to the first memory**, said system** comprising:

a second memory associated with the second data processing unit; and

a mechanism that allows the first data processing unit to offer the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system **so that the second data processing unit does not access the second memory during reduced power mode when the first memory can service the second data processing unit**.

14. (Previously presented) A data processing system as claimed in Claim 13, wherein the second memory unit can be accessed by system components other than the first or second data processing units in the reduced-power mode.

15 (Currently amended) A ~~data processing system as claimed in Claim 13,~~ **A data processing system which may be situated in a reduced-power mode having a first data processing unit that has access to a first memory associated with the first data processing unit and a second data processing unit that has access to the first memory comprising:**

a second memory associated with the second data processing unit; and

a mechanism that allows the first data processing unit to offer the second data processing unit access to the memory belonging to the first data processing unit in a reduced-power mode of the data processing system,

wherein the first data processing unit is arranged for offering the second data processing unit access to the first memory when the second memory is switched off.

16. (Previously presented) A system as claimed in Claim 13, wherein the memory belonging to the first data processing unit forms part of the first data processing unit.

17. (Previously presented) A system as claimed in Claim 13, wherein the memory belonging to the first data processing unit is a cache memory.

18. (Previously presented) A system as claimed in Claim 13, wherein the first data processing unit is a microprocessor.

19. (Previously presented) A system as claimed in Claim 13, wherein the second data processing unit is a video controller.